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10/521,881	09/28/2005	Stefan Marco Koch	CH 020024	8855

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Continuation of 11: NOTE:

Applicant's arguments filed 26 January 2009 have been fully considered but they are not persuasive.

Applicant argues that there is no motivation to combine the teachings of Koch and Tang to arrive at the claimed system.

However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the dual DMA channel interfaces taught by Tang in each of the programmable units taught by Koch, including using the clock domain of each associated processor for the associated DMA interfaces. The motivation for doing so, as provided by Tang, would have been that the second DMA channel interface provides a DMA channel request for a next upcoming DMA transfer, before the current DMA transfer is completed, and initiating set up of the second transfer before the completion of the first, to reduce the latency due to set up time between DMA transfers (column 2, lines 42-55).

In response to applicant's argument that the references may motivate adding a second direct memory access channel interface on the same clock, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Applicant also argues that Koch and Tang do not teach first and second bi-directional channels, the first bi-directional channel being coupled through a first programming interface to a second processor and the second bi-directional channel being coupled through a second programming interface to a first processor.

However, Koch teaches a communication channel for transferring information can be established between the first shareable unit and the second processor and between the second shareable unit and the first processor (paragraph 0051).

/Eddie P Chan/
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